113 2019 Exam La Roon size Zi J bits

b The design of a single ROM and register is based on

finite state machine The Rom is used to remember the combination of controling signals in each state Hence the size of Rom is In X h bits

c

t.eeIzm

s.gf2S.n Total size of Rooms

ControlUnit Controlling State Roomsize signalRom size d THEY

E t

clock 0 Signa

2 Multiplexer selecting bits

Total size of ROMs 2M S t 2M S t zs.cn 12

e Fie sigal Ronasize 2Mt St 25 Ln 12

Za

edxhere doesnotrepresent the variable x It'sJust a storage for the value 3A

b110A x 4 y x b y 1 3a X Zy

b

01110 Sixteen I 110 12.0 00010 0 001 0.25 Normalized

00110 0 011 01001 I too 3.0 01010 0 Lol 4.0

C i The cache can hold 16 floats 1281 8 16

Ii The cache has two sets I I see I b set 2 iii when executing the first iteration of the

loop the code is asking for A63 which

loop e co cg ch is not in the cache and hence this is a miss Thus At uA 3 are loaded in set 1 Then the code is asking for A463 which is again not in see11 set 2 Thus A463 A49 are loaded in set 21 see I No miss would happen up to AED and A493 When accessing AED and Ako there would be a miss The situation occurs later as well so i Miss rate IV Compulsory misses cold misses and capacity miss v The code exhibits spatial locality since it

accesses consecutive elements in A